3D Integrated eWLB /FO-WLP Technology for PoP & SiP

by

Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and *Seung Wook Yoon
STATS ChipPAC Pte Ltd. 5 Yishun Street 23, Singapore 768442
***STATS ChipPAC Pte Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059**

Originally published in the 17th International Conference on Electronic Packaging Technology (ICEPT) 2016, Wuhan, China, Aug 16 – 19, 2016.

3D Integrated eWLB /FO-WLP Technology for PoP & SiP

Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and *Seung Wook Yoon
STATS ChipPAC Pte Ltd. 5 Yishun Street 23, Singapore 768442
*STATS ChipPAC Pte Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059
seungwook.yoon@statschppac.com

Abstract

The trends for smartphone and other mobile devices are more than ever for integration and lower cost. Meanwhile, a higher degree of functionality and performance, thinner profile, and longer battery life are some of the additional market drivers seen in these devices. The implications of these market drivers on the packaging content of mobile devices including internet of things (IoT) and wearable electronics (WE) are; higher performance designs, lower power consumption, lower cost, smaller form factor, thinner profile and higher level of integration.

The emerging of advanced of silicon node technology down to 7/10 nanometer (nm) in support of higher performance, bandwidth and better power efficiency in mobile products push the boundaries of emerging packaging technologies to smaller form-factor packaging designs with finer line/spacing as well as improved thermal electrical/performance and integration of SiP or 3D capabilities. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations.

This paper reports developments that extend multi-die, 3D PoP and 3D SiP applications with eWLB/FO-WLP technology, including ultra thin devices or/and with an interposer substrate attachment. Test vehicles have been designed and fabricated to demonstrate and characterize these low profile and integrated packaging solutions for mobile products including IoT/WE and MEMS/Sensor. Assembly process details and mechanical reliability characterizations are to be discussed with component and board level reliability results. Innovative structure optimization that provides dual advantages of both height reduction and enhanced package reliability are reported. To enable higher interconnection density and signal routing, packages with multi layer RDL and 2/2um fine line/width spacing are fabricated and implemented on the eWLB platform. Successful reliability and electrical characterization results on 3D eWLB-PoP / eWLB-SiP configurations are reported as an enabling technology for highly integrated, miniaturized, low profile and cost effective solutions.

I. Introduction

Newly emerging applications in the consumer and mobile products, the growing impact of the Internet of Things (IoT) and wearable electronics (WE), and the complexities in sustaining Moore's Law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on density scaling and system level integration to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost.

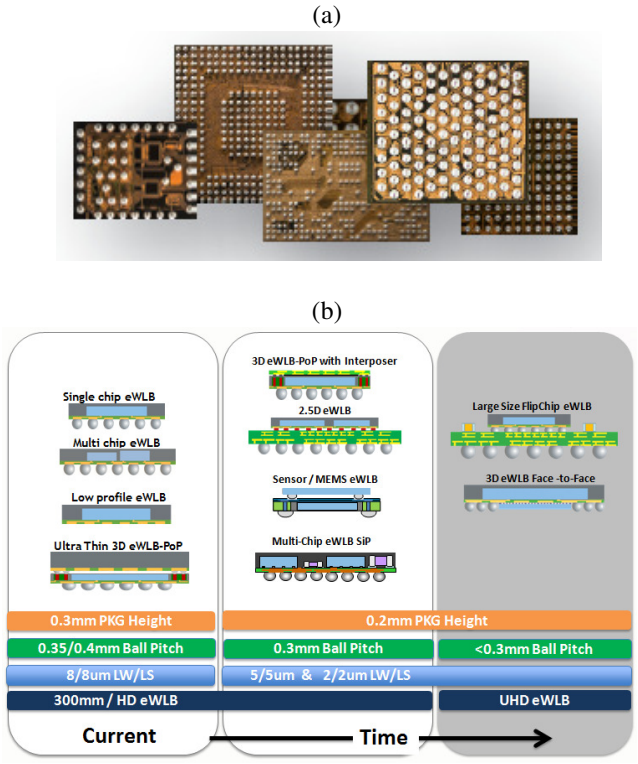

Figure 1. (a) eWLB packages and (b) evolution of eWLB technology from 2D to 2.5D/3D packaging solution

This paradigm shift from chip scaling to system-level scaling is and will continue to reinvent microelectronics system packaging, drive increased system bandwidth and performance, and help sustain Moore's Law. Demand for maximum functional integration in the smallest and thinnest package will continue to growth with an order-of-magnitude requirement for lower manufacturing cost and reasonable cycle time. The challenge of the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals in timely manners.

To meet the above said challenges, eWLB/FO-WLP is a continually evolving technology platform which offers additional space for routing higher I/O chips on top of the silicon (Si) chip area which is not possible in conventional wafer level packaging (WLP) or wafer level bump (WLB)

[1]. Figure 1 shows the eWLB packages and package evolution to 2.5D and 3D SiP. It also offers comparatively better electrical, thermal and reliability performance at a reduced cost with the possibility to address more Moore (advanced technology nodes with low-k dielectrics in SoC) and more than Moore (heterogeneous integration of chips with different wafer technology as SiP solution in multi die or 3D eWLB approaches) as shown Figure 1(b).

eWLB (embedded Wafer Level BGA) Technology

eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency) [2]. The obvious solution to the challenges was some form of WLP. Two choices presented themselves: Fan-in or Fan-out. With Fan-in WLP or Wafer Level Chip Scale Packaging (WLCSP), the I/O density is limited to the die size. In Fan-out WLP (FO-WLP) or eWLB,, the interconnection system is processed directly on the wafer and the I/O density is unconstrained by die size, making it compatible with motherboard technology pitch requirements.

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging[1]. Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLP. Following singulation, the diced silicon wafers are then reconstituted into a standardized wafer (or panel) shape for the subsequent process steps. The reconstitution process as shown on Figure 2 includes four main steps.

1) The reconstitution process starts by laminating and adhesive foil onto a carrier.
2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.
3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.
4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [3].

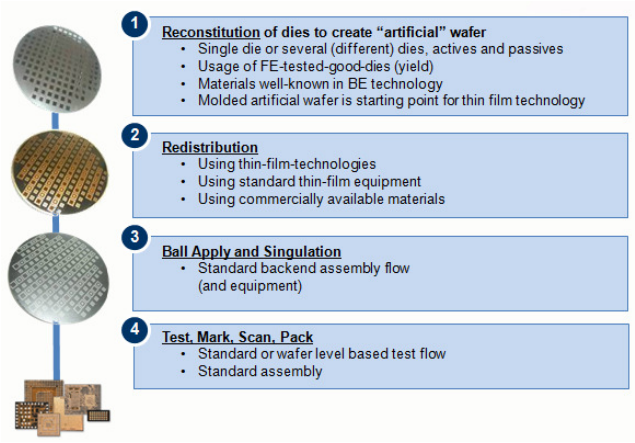

Figure 2. Process flow of eWLB assembly

II. Integrated eWLB Technology

3D eWLB-PoP

The continued demand for higher level of integration has led to the industry's adoption of 3D packaging technologies and, in particular, the Package-On-Package (PoP) configurations. This technology allows for vertical integration of the memory package and the logic package into one stacked package.

Table 1. Value proposition of eWLB-PoP

1. *PoP packages larger than 15x15mm have been enabled using eWLB HVM processes*
2. *Ultra Thin PoP solutions of 0.8mm total stacked package (300um total bottom package thickness with embedded high density vias).*
3. *Further 0.6mm PoP total stacked height, with top memory package made thinner in eWLB technology.*
4. *Package meets all Component Level and Board Level Reliability Tests per JEDEC Standard*
5. *Enhanced thermal and electrical performance with shorter interconnection length compared to flipchip or WB solutions*
6. *Well controlled warpage for thinner package height*
7. *Top ball pitch is scalable down to 0.2mm (~ 1000 I/O in 16x16mm PKG)*
8. *Pre-stacked assembly option available for top package*

The top package is primarily a memory module including some combination of Flash and DRAM, while the bottom package typically contains the logic die, which is a baseband or an application processor of some kind. Top and bottom package are connected via the pads that are located on the top side of the bottom PoP package, and these pads are used to connect the top PoP (memory module) Ball Grid Array (BGA) solder balls to the bottom PoP package. There are various PoP package types including bare-die PoP,

Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand [4].

3D eWLB-PoP offers significant advantages in thin profiles and lower cost compared to current PoP technologies, particularly for mobile or tablet applications. 3D eWLB-PoP bottom has a 300um package height enabling a total stacked PoP height to be less than 0.8 mm after top memory package stacking (body thickness of 0.40mm). Table 1 shows value proposition of 3D eWLB-PoP technology [5].

Electrical Performance of 3D eWLB-PoP and fcPoP

The RLC parasitic values for eWLB-PoP and fcPoP were extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each packages were extracted by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters. The simulation modeling design was carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins were selected and studied, such as clock, VDD as well Data pins.

Table 2. Electrical parasitic values of RL of eWLB-PoP and fcPoP @ 1GHz. :

Net	Inductance, L (nH)			Resistance, R (mΩ)		
	fcPoP	eWLB -PoP	Δ (%)	fcPoP	eWLB -PoP	Δ (%)
1	1.77	0.43	-76%	240	67	-72%
2	2.03	0.24	-88%	308	42	-86%
3	1.51	0.57	-62%	348	112	-68%
4	1.08	0.25	-77%	268	66	-75%

For signal integrity study with specific data pins, eWLB showed more than 10dB better cross-talk than flipchip due to its thinner Cu RDL and overall shorter interconnection length as shown Figure 3. Also smooth Cu RDL surface of wafer fab process contributed significantly with less conductance loss.

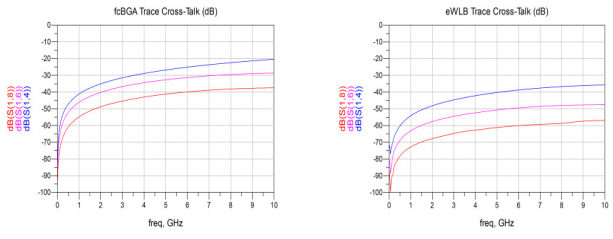

Figure 3. The cross-talk with frequency of signal routing of (a) flipchip and (b) eWLB.

Board Level Reliability of 3D eWLB-PoP/SiP

For board level reliability tests, eWLB-PoP (stacked with top package) was pre-stacked with top memory and mounted on the PCB. For PoP assembly, 0.4mm body thickness FBGA top packages were assembled separately with standard wirebonding process and finally pre-stacked on eWLB-PoP bottom package. Total eWLB-PoP stacked package height was less than 0.8mm in height after SMT on PCB. Those samples were tested in JEDEC TCoB and drop reliability test conditions.

Table 4 shows 3D eWLB-PoP board level reliability of JEDEC TCoB and drop test results of test vehicle 1 and 2 (Table 2 and Figure 3). The first TCoB failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP.

Table 3. Board Level Reliability Test Results of 3D eWLB-PoP/SiP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

2/2um Line Width and Spacing with 3-L RDL [6]

One of the greatest challenges facing wafer level packaging at present is the availability of routing and interconnecting high I/O fine pitch area array. RDL (redistribution layer) allows signal and supply I/O's to be redistributed to a footprint larger than the chip footprint in eWLB. Required line widths and spacing of 2/2 µm for eWLB applications support the bump pitch of less than 40um. Finer line width and spacing are critical for further design flexibility as well as electrical performance improvement. For die-to-die interconnects of high I/O or multi channels, finer line is critical for multi-die design and routing flexibility.

Figure 4 show 2/2um LW/LS RDL in eWLB/FO-WLP. Micrographs show uniform and well defined micro structure. Cu RDL thickness and CD are also well controlled. Even with mixed design of finer and coarse LW/LS. With this process development, it is verified of robust process of fine RDL fabrication using current HVM equipments and process flow.

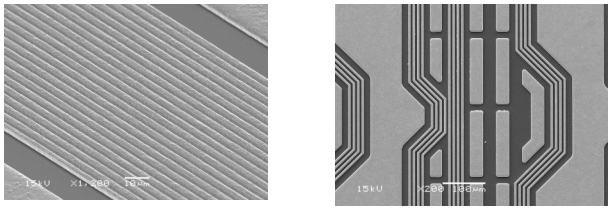

Figure 4. SEM micrographs of 2/2um LW/LS RDL.

3D eWLB SiP / Module

eWLB/FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP

integration is also a growing trend for advanced application processors, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[6].

Figure 5 shows 3D eWLB SiP/module which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB-PoP to form a 3D SiP/ module with a thin package profile of total height of 1.0mm. 12 discretes of inductor and capacitors MLCC were removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. These discretes are also more power effective when they are close to the device, which significantly improves the overall electrical performance as well as provides a power saving advantage.

Functional test sample was prepared with power management integrated circuit (PMIC) as shown in Figures 5. It was a 6x6mm package size with a 4x4mm Si die and 12 discretes on top. This 3D eWLB SiP demonstrated more attractive power efficiency performance compared to other embedded package technology and it is representative of a significantly smaller packaging solution.

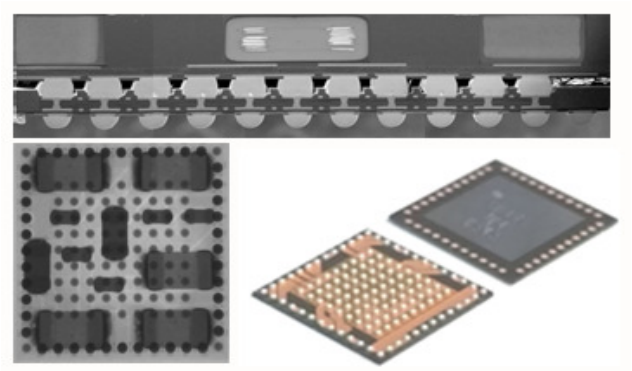

Figure 5. Photographs of 3D SiP eWLB-PoP with discretes on interposer or top package of discretes.

MEMS/Sensor eWLB

eWLB/FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, RF module, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[7].

Figure 6 shows eWLB sensor which has miniaturized from original side-by-side LGA package. It has 3D vertical interconnection and multi-die stacking. It provides over 20% footprint reduction and less than 1mm thickness with lower cost HVM solution. The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors. Since sensor devices typically require at least a two chip solution (ASIC and MEMS/sensing silicon), advanced eWLB/FO-WLP stack-up solutions can enable a very small pitch land-grid array (LGA) and ball-grid array (BGA) eWLB-PoP footprint at a competitive cost vs. the incumbent wirebond solutions. The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard leadfree wafer processing, singulated and assembled by pick-and-place and reflow on the ASIC in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity, removing the typical laminate or leadframe for routing. Therefore, 3D eWLB SiP offers a much smaller footprint, simplified bill of material (BOM), assembled with a cost competitive panel level manufacturing process [8].

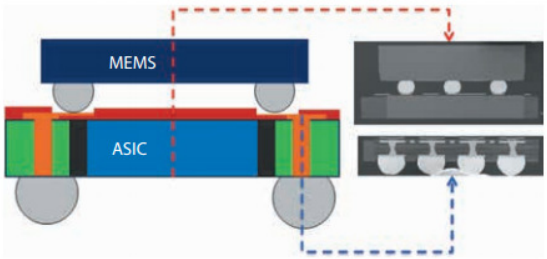

Figure 6. 3D eWLB for MEMS/Sensor Devices[8].

III. Conclusions

Wafer level technology effectively accommodates new foundry technology nodes and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher bandwidth, ultra high density, embedded capabilities, and improved thermal dissipation in a small, thin package format, advanced wafer level packaging is an alternative for flip-chip and leaded packages and is becoming choice in the evolving market. eWLB/FO-WLP technology also provides the ability to tightly manage the co-design process and achieve silicon design optimization, which is significantly critical in ultra cost-sensitive markets.

Advanced low profile and integrated 3D eWLB-PoP/SiP was developed using eWLB (FO-WLP) technology. 3D eWLB/SiP passed JEDEC standard component level reliability conditions. Board level reliability tests of pre-stacked PoP were carried out in JEDEC standard condition and showed robust reliability in TCoB and drop tests both. The electrical characterizations were also carried out with functional devices and signal integrity simulation, and showed the enhanced performance of 3D eWLB-PoP compared to conventional fcPoP.

Advanced 3D eWLB technology provides more smaller form-factor, performance value add and is proving to be a new 3D SiP packaging platform that can expand its application range to various types of emerging mobile, IoT and WE applications including sensors/MEMS or automotive applications.

References

[1] M. Brunnbauer, et al., “Emberdded Wafer Level Ball Grid Array (eWLB),” Proceedings of 8th Electronic Packaging Technology Conference, 10-12 Dec 2009, Singapore (2006)

[2] Seung Wook YOON, Meenakshi PADMANATHAN, Andreas BAHR, Xavier BARATON and Flynn CARSON, “3D eWLB (embedded wafer level BGA) Technology: Next Generation 3D Packaging solutions,” San Francisco, Proceedings of IWLPC 2009 (2009).

[3] Meenakshi Prashant, Seung Wook Yoon, Yaojian Lin, and Pandi C.Marimuthu, “Cost effective 300mm large scale eWLB (embedded wafer level BGA) Technology,” Proceedings of 13th EPTC 2011, Singapore, Dec (2011).

[4] Hamid Eslampour. SeongMin Lee. SeongWon Park. TaeKeun Lee, InSang Yoon, VoungChuI Kim, "Comparison of Advanced PoP Package Configurations. Proce", Proceedings of ECTC 2010, Rino, US (2010).

[5] Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi and Seung Wook Yoon, “Advanced 3D eWLB-PoP (embedded Wafer Level Ball Grid Array - Package on Package) Technology”, Proceedings of ECTC 2016, Las Vegas, US (2016).

[6] W.K. Choi, D.J. Na, K.O. Aung, Andy Yong, Jaesik Lee, Urmi Ray, Riko Radojcic, Bernard Adams and Seung Wook Yoon,”Ultra Fine Pitch RDL Development in Multi-layer eWLB (embedded Wafer Level BGA) Packages”, Proceedings of iMAPS 2015, Orlando, US (2015).

[7] Seung Wook Yoon, Boris Petrov, Kai Liu, “Advanced wafer-level technology: enabling innovations in mobile, IoT and wearable electronics” , Chip Scale Review, May/June 2015, pp54-57(2015).

[8] Babak Jamshidi, “Fan-Out Wafer Level Packaging enables MEMS and Sensors to meet Future IoT Requirements”, MEPTEC Report Summer 2016, p23-24, meptec.org (2016).